

Synthesis and Testing of Reversible Multiplier

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Abstract—Reversible logic is emerging as a promising computing paradigm having its applications in low power VLSI design, quantum computing, nanotechnology, and optical computing. In this paper, a new 4×4 reversible gate termed as SPT gate is proposed, suitable for synthesizing reversible combinational circuits. SPT can also work singly as a reversible full adder with only two garbage outputs. A 4×4 multiplier synthesized using SPT gates is found to have minimum number of garbage outputs when compared to the multiplier designed with Peres gates. Stuck-at fault (SAF) model is widely used for testing conventional CMOS circuits and new fault models, namely single missing-gate fault (SMGF), repeated-gate fault (RGF), partial missing-gate fault (PMGF), and multiple missing-gate fault (MMGF) have been found to be more suitable for modeling defects in quantum gates. In this paper it is shown that in an $(n \times n)$ reversible circuit implemented with SPT gates, addition of only one extra control line along with duplication of each gate yields an easily testable design, which admits a universal test set of size $(n+1)$ that detects all SMGFs, RGFs, PMGFs, and MMGFs in the circuit.

Keywords— Multiplier, Fault Models, Reversible Logic, Testable Design, Universal Test Set

I. INTRODUCTION

In VLSI circuit design, where power dissipation plays an important role, there has been an increasing trend of packing more and more logic elements into smaller and smaller volumes and clocking them with higher frequencies. Reversible logic is emerging as a promising computing paradigm having its applications in low power VLSI design, quantum computing, nanotechnology, and optical computing [3],[4],[5],[6]. The logic elements are normally irreversible in nature and according to Landauer's principle [1] irreversible logic computation results in energy dissipation due to power loss. This is because, erasure of each bit of information dissipates at least $KT \ln 2$ joules of energy, where K is Boltzmann's constant and T is the absolute temperature at which the operation is performed. By 2020 this will become a substantial part of energy dissipation, if Moore's law continues to be in effect. Feynman and Bennet realized this particular problem of VLSI designing in 1970s. In 1973 Bennet [2] had shown that energy dissipation problem of VLSI circuits can be circumvented by using reversible logic.

This is because reversible computation does not require erasing of any bit of information and consequently it does not dissipate any energy for computation. Reversible computation requires reversible logic circuits and synthesis of reversible logic circuits differs significantly from its irreversible counterpart because of different factors [4]. In an n -output reversible gate, the output vectors are permutations of the numbers 0 to $(2n - 1)$. Logic synthesis using reversible gates should have [14] minimum number of reversible gates and constant inputs, and produce less garbage outputs.

Reduction of these parameters is the bulk of the work in reversible circuit design. Reversible circuits for different purposes e.g. half adder, full adder and multiplier [12], [13], [8] have been proposed recently. Among these reversible circuits, multiplier circuits are of special importance because of the fact that they are the integral components of every computer system, cellular phone and most digital audio/video devices. It is important for every processor to have a high-speed multiplier. Multiplier circuits essentially have two components: partial product generator and parallel full adder. In this paper, we aim to provide a testable design for a reversible full adder and multiplier with optimized garbage outputs and constant inputs.

The rest of the paper is organized as follows: In section 2, the details of the SPT gate and its use as full adder are given. Different fault models are described in section 3. Testable design of the gate for detecting stuck-at and missing-gate faults using universal test vector is provided in section 4. Section 5 gives the synthesis of multiplier with SPT gate. The CMOS realization of SPT gate is given in section 6. The results are given in section 7 and finally section 8 concludes the paper.

II. SPT GATE

Testing of a reversible circuit, in general, turns out to be relatively simpler compared to that of non-reversible logic because of inherent ease of controllability of logic states and observability of errors. Another important property that expedites the test generation process is the fact that back tracking is straightforward and always yields a unique vector at the input.

The block schematic of SPT gate shown in figure 1 is having 4 inputs and 4 outputs. The quantum representation and full adder block using this gate are also shown in the figure.

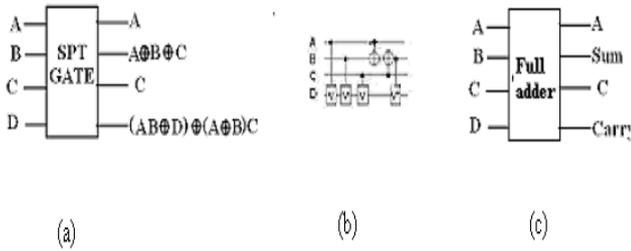


Fig. 1. SPT Gate (a) Block schematic, (b) Quantum implementation, and (c) As full adder block

The quantum cost of SPT gate is 6. If input $D=0$ then this gate acts as a full adder. Figure 2 shows quantum representation of full adder using SPT gate.

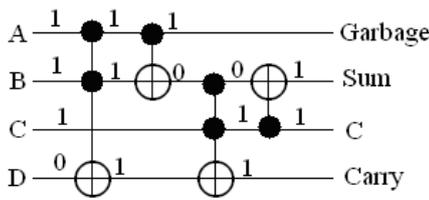


Fig. 2. Quantum representation of full adder

III. FAULT MODELS

Several fault models for SPT gate and their detection by using universal test vector are explained in this section. These are Stuck-at Fault (SAF), Single Missing-Gate Fault (SMGF), Repeated-Gate Fault (RGF), Partial Missing-Gate Fault (PMGF), and Multiple Missing-Gate Fault (MMGF) models.

A. Stuck-at Faults (SAF)

A stuck-at fault is a particular fault model used by fault simulator tools to mimic a manufacturing defect within a reversible circuit. Individual signals and pins are assumed to be stuck at logical '1' or '0'. For example, an output is tied to a logical 1 state during test generation to assure that a manufacturing defect with that type of behavior can be found with a specific test pattern. Likewise the output could be tied to a logical 0 to model the behavior of a defective circuit that cannot switch its output. Not all faults can be analyzed using the stuck-at fault model. Figures 3(a) and 3(b) shows the examples for stuck-at 1 and stuck-at 0 faults respectively.

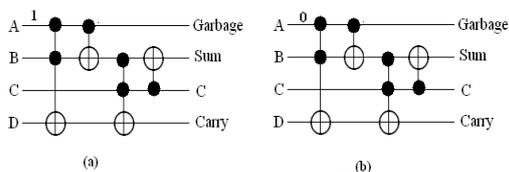


Fig. 3. (a) Stuck-at 1 fault and (b) Stuck-at 0 fault

B. Single Missing-Gate Faults (SMGF)

A single missing-gate fault [5] is defined as a complete disappearance of one CNOT gate from the circuit. The physical justification for a SMGF is that the pulse(s) implementing the gate operation is (are) short, missing, misaligned or mistuned. Figure 4 shows the SMGF, where the first 2-CNOT gate is missing.

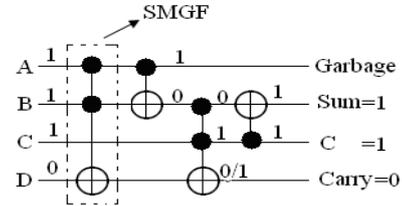


Fig. 4. Single missing-gate fault

SMGF is detected by setting logic 1 value on all the control inputs of the gate, and any value, either 0 or 1 on the target input as well as on the wires not connected to the gate. In the example of figure 3, if we apply $\{A,B,C,D\} = \{1,1,1,0\}$ at the input of the circuit, the normal output would be $\{P,Q,R,S\} = \{1,1,1,1\}$, whereas, in the presence of the SMGF fault marked by the dotted box, the output will be $\{P,Q,R,S\} = \{1,1,1,0\}$. The number of possible SMGFs is equal to the number of gates in the circuit.

C. Repeated-Gate Faults (RGF)

A repeated-gate fault (RGF) is an unwanted replacement of a k -CNOT gate by several instances of the same gate [5]. An RGF may be needed to model the occurrence of long or duplicated pulses. Figure 5 shows an example, where first gate is repeated in the circuit. The effect of this fault is thus same as that of an SMGF at the first 2-CNOT gate in the original circuit.

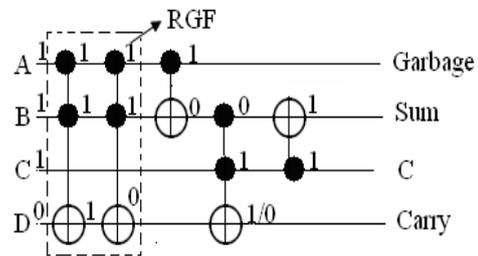


Fig. 5. Repeated-gate fault

If we apply $\{A,B,C,D\} = \{1,1,1,0\}$, the normal output would be $\{P,Q,R,S\} = \{1,1,1,1\}$, whereas, in the presence of the above RGF marked by the dotted box, the output will be $\{P,Q,R,S\} = \{1,1,1,0\}$. Hence, it is detected by the vector $\{A, B, C, D\} = \{1, 1, 1, 0\}$. It is clear that if a RGF replaces a gate by even number of instances of the same gate, its effect is similar to the effect of the SMGF with respect to the same gate. If the RGF replaces a gate by odd number of instances of the same gate, the fault is redundant,

i.e., it does not change the function of the circuit. Further, it has been shown that any SMGF test set detects all detectable RGFs [5].

D. Partial Missing-Gate Faults (PMGF)

This is used to model the defects resulting from the partially misaligned or mistuned gate pulses [5]. It changes a k -CNOT gate into a p -CNOT gate, with $p < k$. The corresponding fault is called as $(k - p)^{th}$ order PMGF. Fig. 6 shows a first-order PMGF. An SMGF can be seen as a 0-order PMGF.

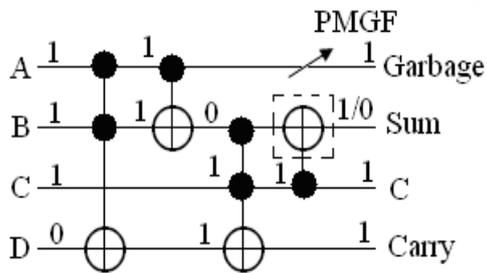


Fig. 6. Partial missing-gate fault

E. Multiple Missing-Gate Faults (MMGF)

This is defined as complete disappearance of two or more consecutive k -CNOT gates from the circuit. In the circuit of figure 7, it is shown that the circuit has an MMGF marked by the dotted box. This fault is detected by the vector $\{A, B, C, D\} = \{1,1,1,1\}$.

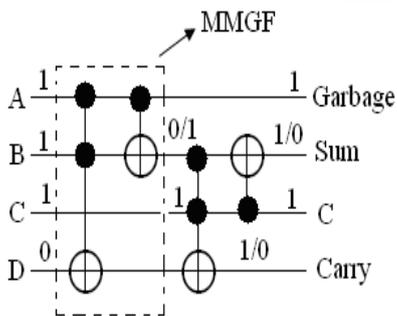


Fig. 7. Multiple missing-gate fault

IV. TESTABLE DESIGN FOR DETECTING FAULTS

An exact ATPG scheme has been reported earlier [5] that generates test vectors for various types of missing gate faults discussed above. The universal test vector for testing a reversible gate is given below.

$$S_U = \begin{pmatrix} x_1 & x_2 & \dots & x_n & c_x \\ 0 & 1 & \dots & 1 & 1 \\ 1 & 0 & \dots & 1 & 1 \\ \dots & \dots & \dots & \dots & \dots \\ 1 & 1 & \dots & 0 & 1 \\ 1 & 1 & \dots & 1 & 0 \end{pmatrix}$$

To detect all PMGFs by a universal test set, adding one wire and duplicate k -CNOT gates augments the original reversible circuit. A first-order PMGF affecting the j th control input can be detected by setting 0 at the j th control input and 1 at all the other

control inputs. For such a vector, the fault-free and the faulty gate will produce different values on the target node. Therefore, to detect all first order PMGFs in a k -CNOT gate as shown in figure 8, we will have to apply the following k test vectors $\{x_1 x_2 \dots x_j \dots x_k\}$, $(0 1 \dots 1 \dots 1 \dots X)$, $(1 0 \dots 1 \dots 1 \dots X) \dots (1 1 \dots 1 \dots 0 \dots X)$ at the input level, where X , applied to the target input may be 0 or 1.

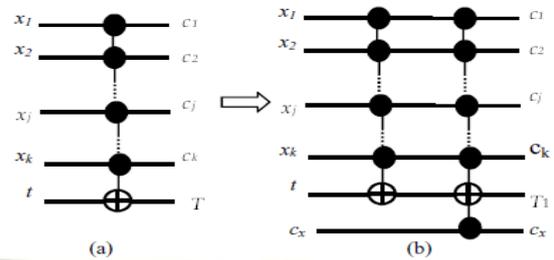


Fig. 8. (a) A k -CNOT gate and (b) Augmented CNOT gate

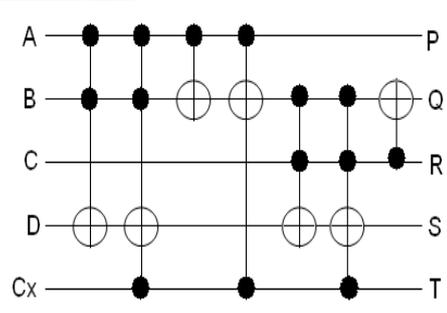


Fig. 9. Augmented SPT gate

Figure 9 shows the augmented reversible SPT gate. An $(n \times n)$ reversible circuit R of depth d is built with a cascade of k -CNOT gates. While the above k test vectors applied at the inputs to R are guaranteed to detect all PMGFs at the first CNOT gate, they may not detect a PMGF at a CNOT gate lying at a subsequent level, as the vectors change when they propagate through various levels. However, if we are able to produce the same k patterns at the inputs of each CNOT gate lying at all other levels, then all PMGFs of first order can be detected in the reversible circuit. To restore the test patterns at each level, we augment a k -CNOT gate as shown in figure 8(b). The same k -CNOT gate is repeated consecutively, and one additional control input c_x is added.

By using the proof proposed in [5] and given below, all the stuck-at-faults and missing-gate faults can be detected. The target output T_1 of the augmented gate is equal to the target input t when $c_x = 1$. This can be explained as follows: The output of the target line

$$T = t \oplus (x_1.x_2 \dots x_j \dots x_k)$$

after augmentation, the target output T_1 when $c_x = 1$ is given by

TABLE I. COMPARISON OF PERFORMANCE PARAMETERS OF VARIOUS MULTIPLIER CIRCUITS

S.No.	Reversible multiplier circuit	Gate count	Quantum cost	Garbage outputs
1.	Proposed	28	168	40
2.	Islam et. al. [14]	94	140	52
3.	Shams et. al. [9]	138	195	56
4.	Thapliyal and Srinivas[8]	138	209	58

CONCLUSIONS

A new gate called SPT gate is proposed and a 4×4 multiplier is synthesized using this gate. The gate is implemented with CMOS transistors and various performance parameters such as gate count, quantum cost, and numbers of garbage outputs are measured for the multiplier. A comparison of these parameters with the available reversible multiplier circuits shows that the proposed multiplier realized with SPT gates gives optimum values of these parameters. This work also presents a design-for-testability technique for testing stuck-at and missing-gate faults. The technique derives a universal test set of length (n+1) for detecting all partial, single, and multiple missing-gate faults along with all detectable repeated-gate faults and stuck-at faults. All SMGFs are tested for a 4×4 reversible SPT multiplier with 100% fault coverage.

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